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DYNAMIC BEHAVIOUR OF TUNNEL DIODE MONOSTABLE CIRCUITS†

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The dynamic behaviour of tunnel diode monostable circuits is analysed as a function of a characteristic circuit parameter. The analysis has been developed in a general way and a special emphasis has been given to the problems of fast nuclear electronics. This analysis refers to circuits with current gain larger than one and to those performing only logic operations. It is also comparative between circuits with linear and non linear biasing. Tunnel diode circuits biased very near to the peak have been regarded with a view to stability for multiple switching; this is in fact the most important limit for high sensitivity monostable circuits. Experimental results have been compared with theoretical calculations.

1. Introduction

The tunnel diode (td) monostable circuit, being simple and easy to realize, is most frequently used as discriminator and shaper and it is the fundamental circuit amongst those capable to perform logic functions at a repetition rate higher than 100 MHz, ref. [1–21]). Its properties have been generally known for a long time[22]).

Particular results have been given with regard to computer logic circuitry, but we are not aware of works of a greater generality whose results may turn out useful in problems of fast nuclear electronics.

The dynamic quantities considered in our analysis depend upon the parameters of the actual circuit and therefore the results are quite different from these published in works regarding the performances of the td alone[23–25]). The analysis has been carried out parametrically for circuits with current gain $G_I > 1$, or $j_0 > 0.55$* and for those performing only a logic function ($G_I < 1$; $j_0 < 0.55$). The dynamic quantities describing in both cases the circuit performance, are the resolution time, the width and amplitude of the output signal. All of these are taken as a function of the characteristic parameter $K = L/(R_p^2 C_1)$. The analysis is comparative between circuits with linear bias (lb) and non linear bias (nlb); the circuits biased with a current near to the I_p value have been included and limits for multiple switching stability in the two biasing conditions, have been calculated. The results carried-out in our analysis have been compared with experimental results published so far by several authors.

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* The current gain G_I is defined as

$$G_I = \{f_T(v_{max}) - j_v\}/j_{in},$$

where:

$f_T(v) = j$ = the td current normalised to the peak current I_p;
v_{max} = the maximum value of the voltage, during the dynamic cycle of the circuit, normalised to the peak voltage V_p;
j_v = the normalised value of the current at the valley point;
j_{in} = normalised input current;
j_0 = normalised biasing current;
K = parameter as defined in section 2.

2. General considerations

The circuits with their equivalent schemes are shown in fig. 1a,b. The td static characteristics (V,I) have been fitted with two parabolic functions[23]) joining at the point $[1.5\ V_p, f_T(1.5\ V_p)]$. The static characteristic (V,I) of the biasing diode in fig. 1b has been fitted with two exponential functions joining at the point $[1.5\ V_p, f_D(1.5\ V_p)]$.

The normalised differential equations are the following:

a. for lb (fig. 1a)

$$\left.\begin{aligned} dv_T/dT &= j_{in} + j_0 + j_L - f_T(v_T) \\ dj_L/dT &= (E - nj_L - v_T)/K \end{aligned}\right\} \qquad (1)$$

the nodal equilibrium equation at point A and the equation for the loop in which the current j_L flows respectively, with: $K = L/(R_p^2 C_1)$; $dT = dt/(R_p C_1)$; $R_p = V_p/I_p$.

b. for nlb (fig. 1b):

$$\left.\begin{aligned} dv_T/dT &= j_{in} + j_0 - f_T(v_T) \\ dv_D/dT &= [j_B - j_L - f_D(v_D)]\,(C_1/C_2) \\ dj_L/dT &= (v_T - v_D)1/K \end{aligned}\right\} \qquad (2)$$

the nodal equilibrium equations at points A, B and the differential relation for the current j_L in the inductance, respectively. The field of variability chosen for K is between 20 and 10^4 being this the only one of practical meaning. The sets of eqs. (1) and (2) have been solved with the aid of a digital computer.

3. Monostables with $G_I > 1$

A set of calculations has been worked out with td biased with $j_0 = 0.9$ which is the maximum value

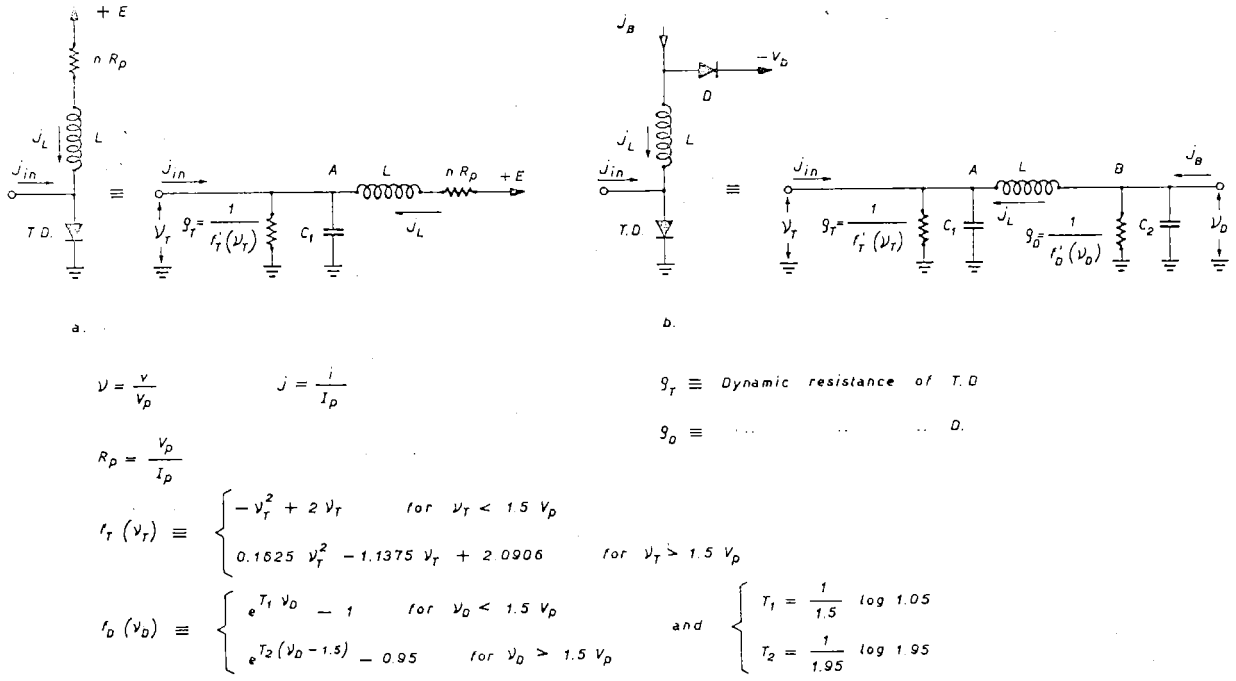


Fig. 1. Tunnel diode monostable schemes; a. linear bias, b. non linear bias.

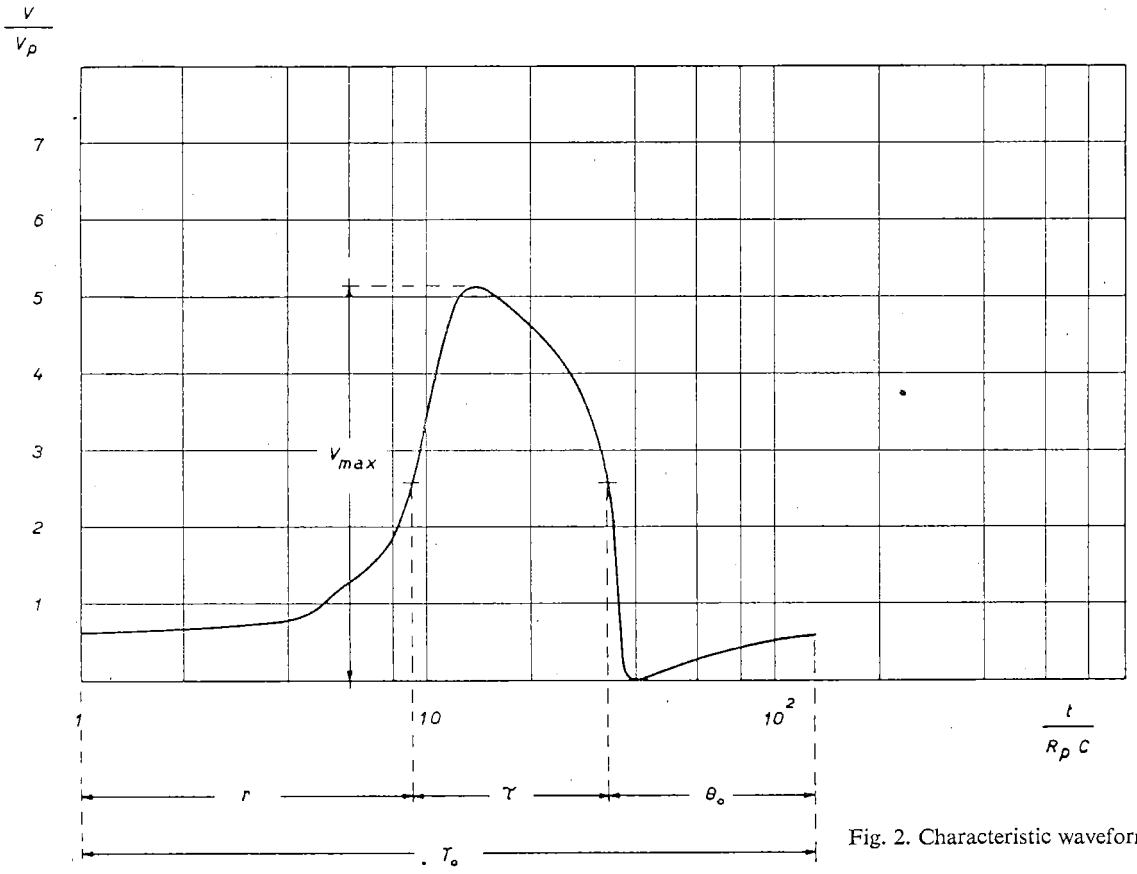


Fig. 2. Characteristic waveform.

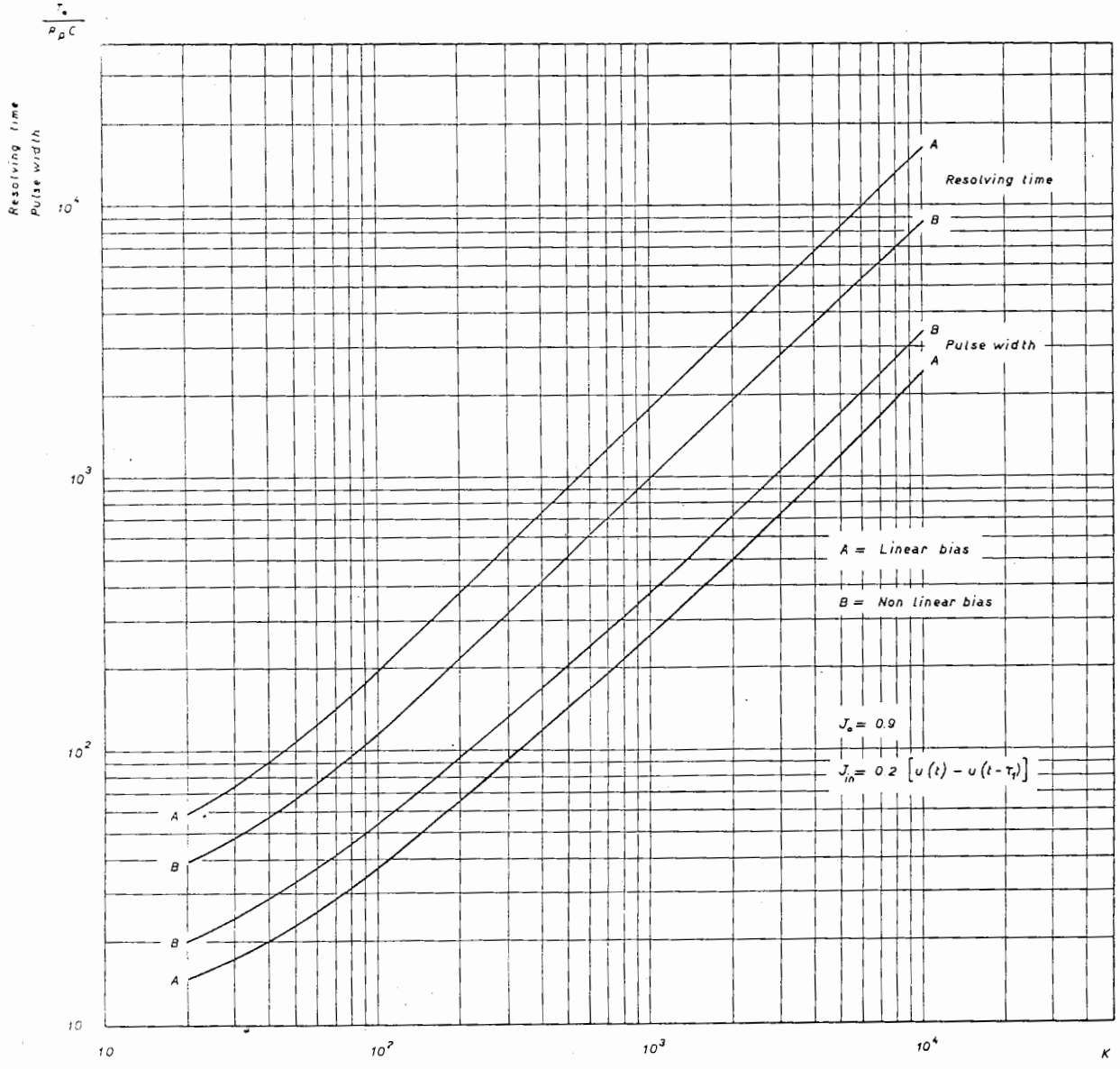


Fig. 3. Resolving time and width vs K.

allowed by tolerance considerations for maximum G_I, ref. [25]). Output waveforms have been obtained for an input triggering pulse $j(t) = j_{in}[u(t) - u(t-\tau_1)]$ where τ_1 is the minimum allowed width to fire the td. For a better understanding of the dynamic quantities we refer in fig. 2 to a typical voltage waveform:

a. T_0 = the total duration of the dynamic cycle (v, j) from the biasing point (v_0, j_0) to the quiescent point $\{v_0 \cdot (1\text{–}0.01), f_T[v_0 \cdot (1\text{–}0.01)]\}$;

b. A_0 = the input pulse amplitude normalized to $I_p[A_0 = j_{in}]$ with 10% overdrive*;

c. τ = the output width measured at fwhm;

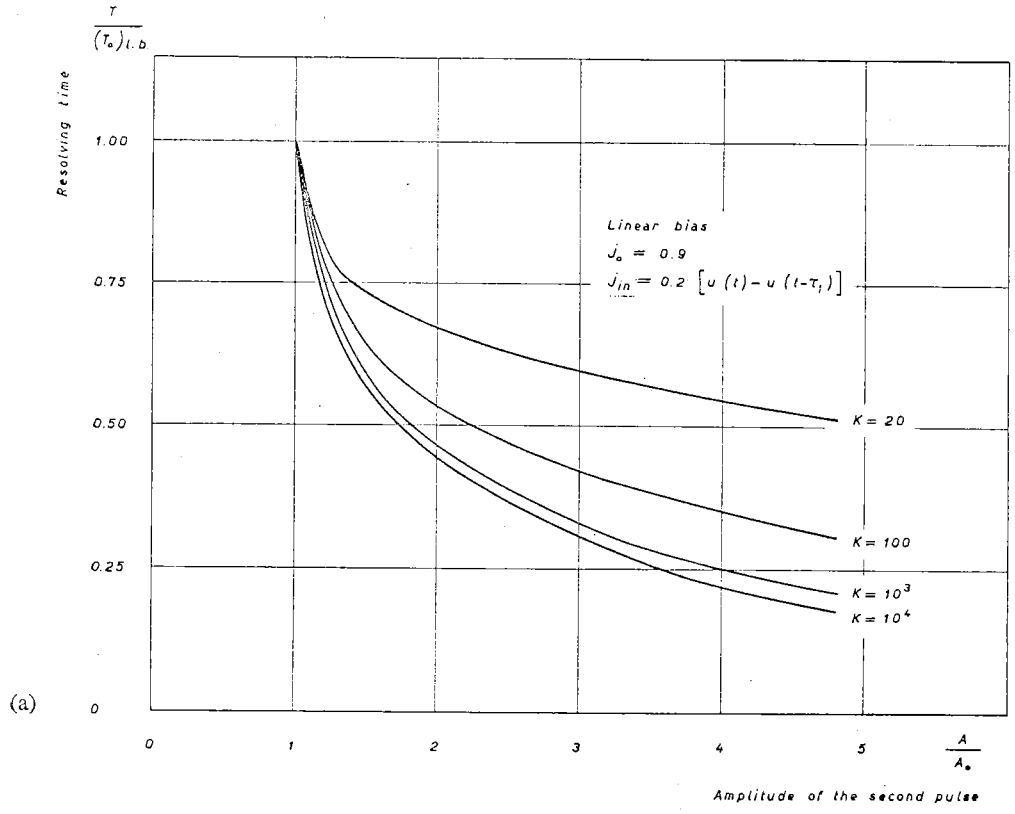
d. θ_0 = the dead time measured on the trailing edge from fwhm to the quiescent point;

e. δ = the duty cycle, defined as: $\delta = \tau/T_0$.

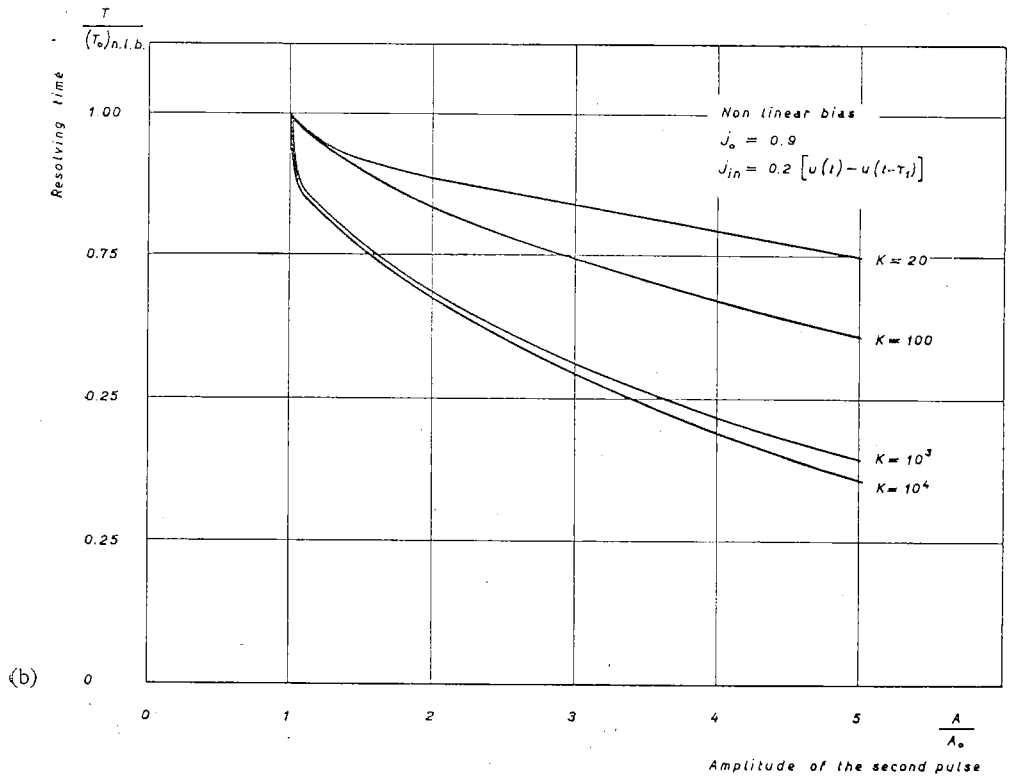
3.1. Resolving time vs K

The resolving time vs K is shown in fig. 3 for lb and nlb. It has been defined $(= T_0)$ as the minimum delay between two equal amplitude input pulses. For $K > 10^2$ the ratio between operation rates for nlb and lb is approximately 1.8.

* Overdrive $= j_{in} + j_0 - 1$.



(a)



(b)

Fig. 4. Resolving time vs amplitude of the second pulse.

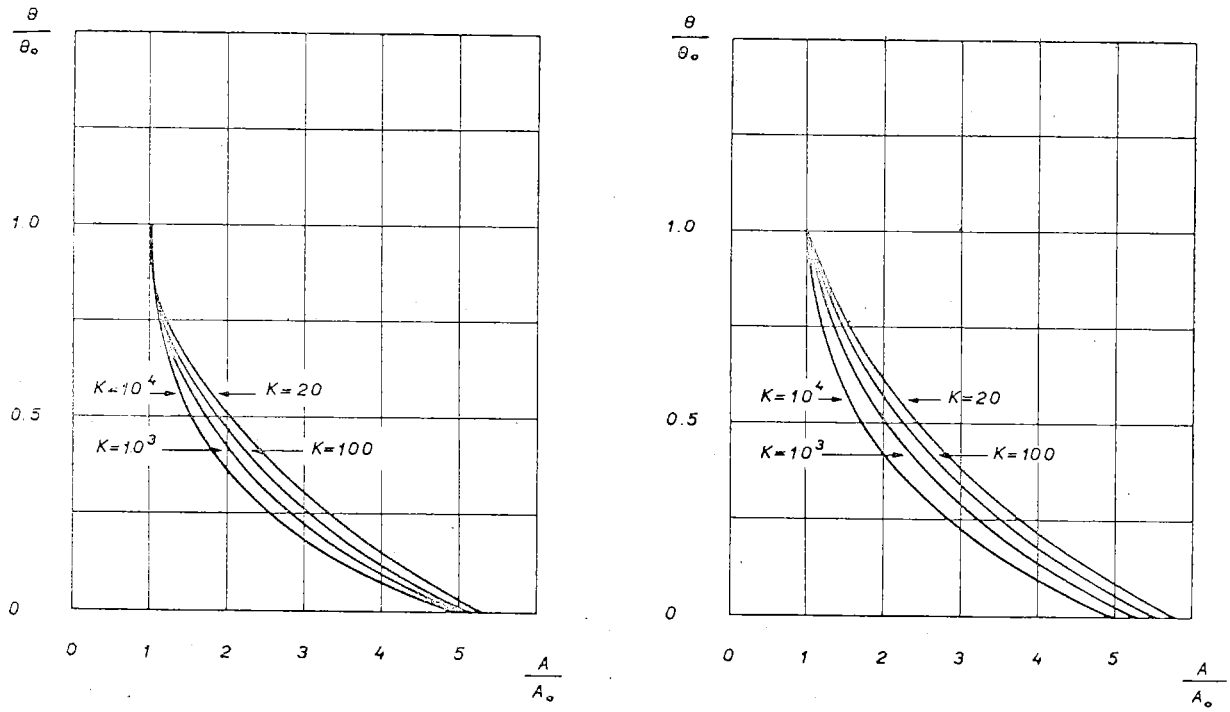


Fig. 5. Dead time vs amplitude of the second pulse; a linear bias; b. non linear bias.

3.2. Output pulse width vs K

For the same value of K the output pulse width (fig. 3) in the case of nlb is always larger than that for lb; the width and the resolving time for nlb are contained between the curves for the lb. This can be summarized saying that the duty cycle is 40% for the nlb and 20% for the lb. For low values of K the curves show a lower value for the duty cycle δ, which is in good agreement with experience. To have the same width, different values of K must be chosen ($K_{nlb} < K_{lb}$). This brings in turn a further increase for the ratio of the operation rates with advantage for the nlb circuit.

3.3. Resolving time vs amplitude of the second input pulse

The diagrams in fig. 4 show the resolving time, T, normalized to T_0, for two input pulses, vs the amplitude of the second input pulse, A, normalised to the amplitude A_0 (0.2 for our case) of the first pulse. The amplitude needed to reduce the resolving time for the nlb is greater than that needed for the lb. In fact the increase of amplitude of the second pulse reduces only the dead time that is already little for the nlb.

The diagram of the dead time θ, normalised to θ_0, for the two cases of biasing, is reported in fig. 5 vs the ratio A/A_0.

3.4. Maximum output pulse amplitude vs K

The output amplitude, normalised to V_p, vs K is shown in fig. 6. The scale factor $S_f = 5.88\ V_p/V_{pp}$* matches the static characteristic (V, I) of the actual td to the ideal one.

The normalised projected peak voltage has been assumed for the calculation as $v_{pp} = 5.88$. It can be noted that for $K = 20$ the output amplitude is nearly equal to the valley voltage v_v, that is the pulse is useless for practical applications. For equal output pulse amplitude the value of K for nlb is lower than that for lb; therefore one can at once deduce that the operation rate for the nlb is higher. With useful output amplitude the circuit with nlb allows to reach an operation rate not otherwise attainable.

3.5. Parameter W vs output signal amplitude

It may be meaningful to consider the product W, (output signal amplitude $\times\ T_0^{-1}$), since it may be taken as a parameter to compare the monostable circuits in the two biasing conditions considered. The plot of W, vs the output signal maximum value, is shown in fig. 7. It is useful to find the value of R_pC_1, that is to choose

* V_{pp} is the projected peak voltage of the actual td.

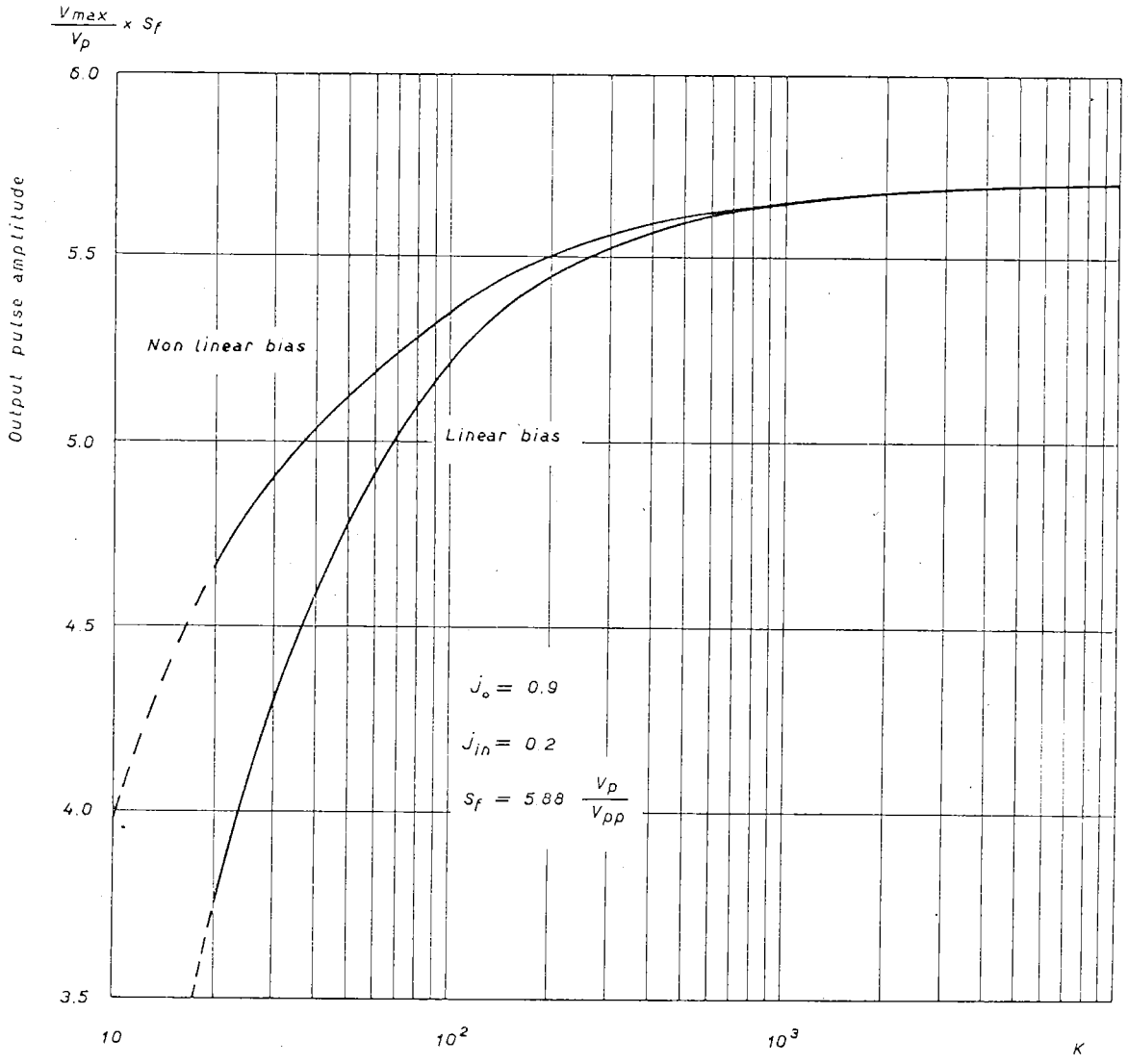


Fig. 6. Output pulse amplitude vs K.

the td. It can then furnish the maximum value of the output signal obtainable when the operation rate has been fixed.

4. Monostable circuits with $G_I < 1$

We have considered the biasing conditions $j_0 = 0$ and $j_0 = -1$. In these conditions it is impossible to find a point* on the negative resistance region of the td where a switching regenerative action may continue once the input current has been removed. Infact the j_L current is, in each point, lower than that needed by the td.

* This point is defined by the following relations:

$$d(j_{in} + j_L)/dv_T = df_T(v_T)/dv_T; \quad j_L > f_T(v_T).$$

The input waveforms may be represented by:

$$j(t) = j_{in}[u(t) - u(t-\tau_2)],$$

where τ_2 is the input pulse width which is maintained as long as the output voltage is risen to its maximum. The dynamic quantities have been gathered in table 1 for lb and in table 2 for nlb. Generally we can say that, when j_0 is lowered, the voltage step across the inductance increases. As a result, when $j_0 < 0.55$ ($G_I < 1$) the output pulse width depends from the circuit (K) but strongly from the biasing point, so that the signal width becomes very short. If the input signal is longer than τ_2, the circuit behaves as that with $G_I > 1$. In fact the input current must be added to the biasing one.

TABLE 1
Linear bias, for $j_0 = 0$ and $j_0 = -1$.

	K	Maximum amplitude (V_p)	Rise time (R_pC_1)	Width (R_pC_1)	Dead time (R_pC_1)	Resolution time (R_pC_1)
$j_0 = 0$	20	–	–	–	–	–
	10^2	5.43	18	10.6	2.3	25
	10^3	5.90	18	16.9	5.6	32
	10^4	5.96	18	22.2	7.8	39.4
$j_0 = -1$	20	–	–	–	–	–
	10^2	5.76	11.6	8.8	1.9	15.2
	10^3	5.89	16.7	9	2.6	21.5
	10^4	5.96	18.2	10.9	3	23.5

TABLE 2
Non-linear bias, for $j_0 = 0$ and $j_0 = -1$.

	K	Maximum amplitude (V_p)	Rise time (R_pC_1)	Width (R_pC_1)	Dead time (R_pC_1)	Resolution time (R_pC_1)
$j_0 = 0$	20	5.0	17	7.8	2	22
	10^2	5.62	17	11.4	2.5	25
	10^3	5.9	17	18.8	6	34
	10^4	5.96	17	24.4	8	41.6
$j_0 = -1$	20	4.98	18	6.7	1.5	22
	10^2	5.6	18	8.23	2.1	23.4
	10^3	5.9	18	10.7	2.9	23.4
	10^4	5.96	18	13.2	3	25.8

5. Analysis of the stability for biasing current near to the peak (I_p).

The lowest threshold of a switching circuit is determined by two factors: a. the noise; b. the overshoot after the switching transients, which is as more dangerous as lower is the threshold. We want to calculate the lowest threshold value keeping into account the contribution from the two limitations cited above.

5.1. STABILITY FOR NOISE CURRENT

It is well known[26]) that the intrinsic noise current of a td may be expressed by:

$$i_r^2 = 4kTg_e\Delta f,$$

where:

$$g_e = [r_s + g_d/\{g_d^2 + (\omega C_1)^2\}]^{-1},$$

r_s = the td series resistance;
k = the Boltzmann constant;
g_d = the equivalent conductance of a td at the biasing point.

For $j_0 \simeq 1$, $g_d \geqq 0$. Assuming $r_s = 1\Omega$ we can write:

$$i_r = 2(kT\Delta f)^{\frac{1}{2}},$$

whose value for $\Delta f = 10^{10}$ Hz, $T = 300°$K is 12 μA. Disregarding the effect of the equivalent conductance of the current generator i_r, we see that, in the case of $I_p = 10^{-2}$ A, the highest value allowed for j_0, regarding only the noise limitations, is $j_0 = 0.999$.

For low level discrimination, td with $I_p = 10^{-3}$ A are commonly used. As a result we can hold that, with some safety factor, the highest allowable value of j_0 is 0.99.

5.2. STABILITY OF LB CIRCUITS

On the basis of experimental work[27]) we assume in this case the equivalent circuit of fig. 8a in which:

$R_1 = mR_p$ is the td differential resistance at the biasing point;

C_1 the td capacitance, assumed constant and equal to the value of the td valley capacitance.

The characteristic determinant of the circuit gives, for critical damping, the following condition:

$$(R_1R_2C_1 + L)^2 - 4LR_1C_1(R_1 + R_2) \geqq 0,$$

from which substituting the defined parameters, we obtain:

$$|(\sqrt{K}/m) - (n/\sqrt{K})| \geqq 2. \qquad (3)$$

With the parabolic approximation assumed for the td static characteristic:

$$m = \tfrac{1}{2}(1 - j_0)^{-\frac{1}{2}}. \qquad (4)$$

The relation (3) is plotted in fig. 9a for $n = 2$. It gives the gap of forbidden values of K vs the biasing current. For biasing current $j_0 < 0.99$, which is the noise limit assumed above, we can state that the condition (3) does not impose further limitation for the allowable values of K.

5.3. STABILITY OF NLB CIRCUITS

On the basis of the equivalent circuit in 5.2, linearising the resistance of the biasing diode, we obtain the circuit in fig. 8b. Noting that $R_1C_1 \ll R_2C_2$ we can disregard C_1. As in [27]) we think the inductance as an ideal buffer during the back-switching of the td. We can then assume that the biasing diode is behind the knee of its characteristic and put approximately $R_2 \simeq 30\ R_p$, as we have calculated from the exponential approximation given in fig. 1.

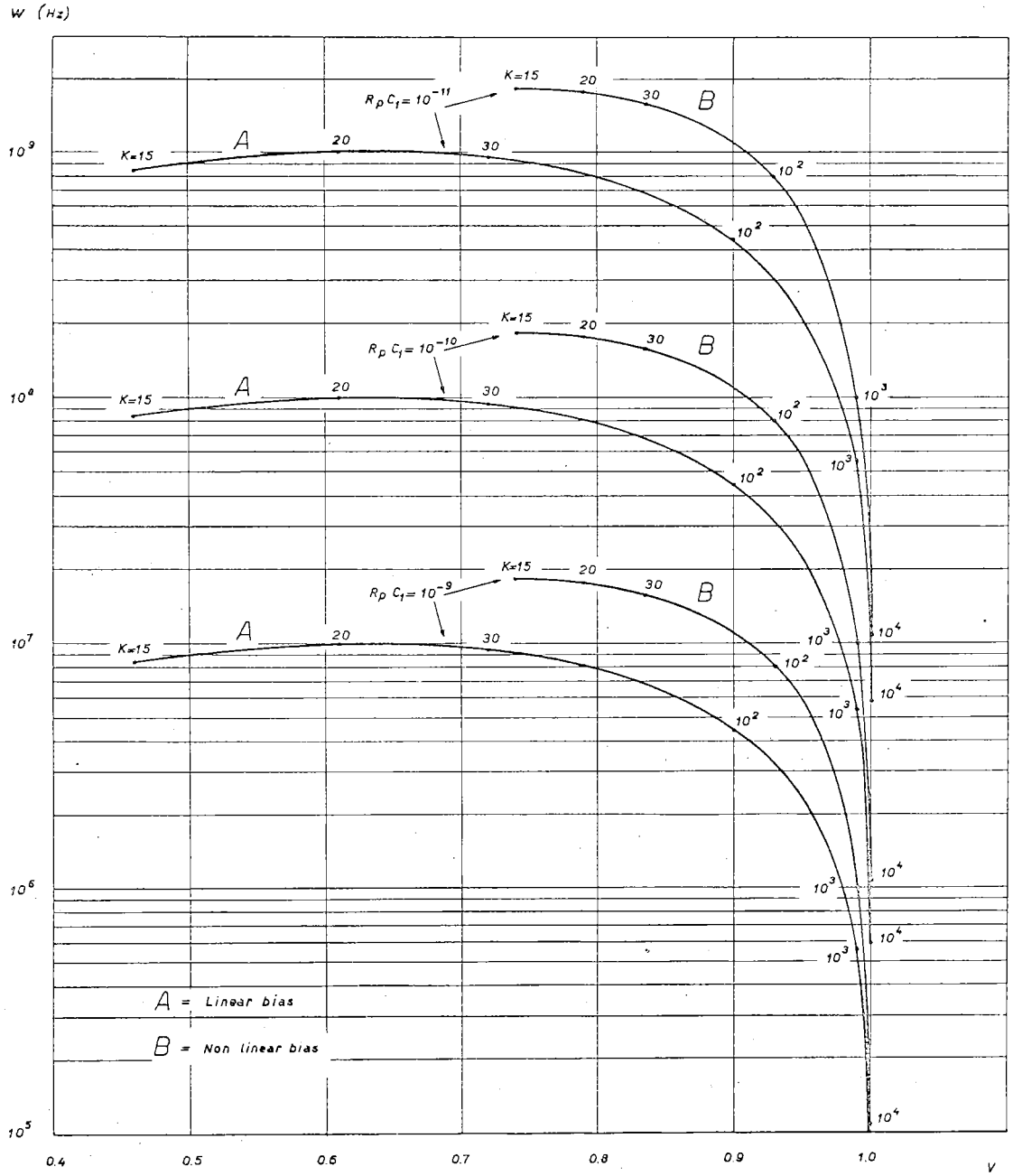


Fig. 7. W factor vs V.

The critical damping condition, the same as (3), is:

$$|(\sqrt{K}/n')-(m'/\sqrt{K})| \geqq 2, \qquad (5)$$

where:

$$n' = n/\sqrt{c}; \quad m' = m/\sqrt{c}; \quad c = C_1/C_2.$$

Regarding eq. (5) we find that the two roots K_1 and K_2 vary proportionally to $1/c$. We can now obtain precise values of m from eq. (4), but the evaluation of

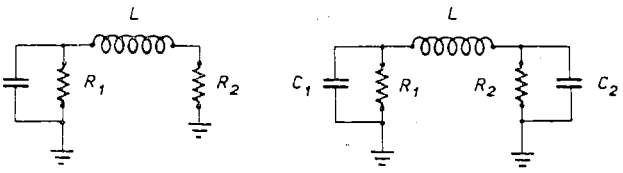


Fig. 8. Equivalent circuit from the idealized characteristics a. linear bias; b. non linear bias.

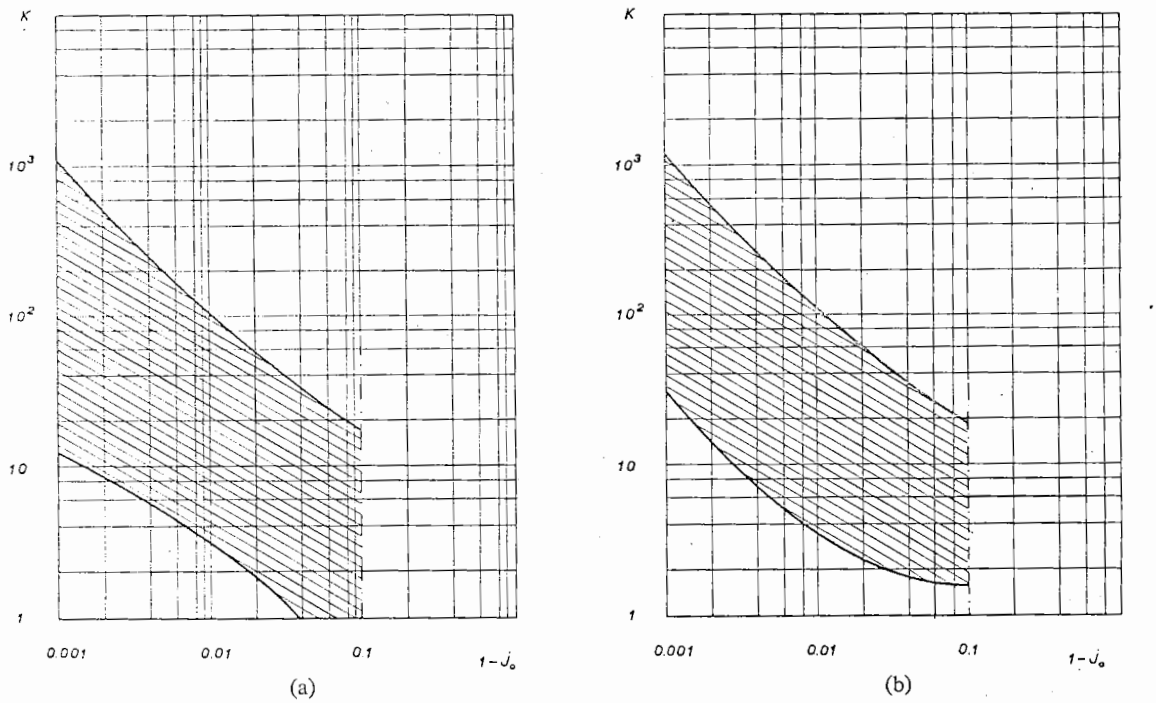


Fig. 9. K forbidden values: a. linear bias; b. non linear bias.

n, vs the biasing current, remains problematic. Since the inductance differs very much from an ideal buffer, the hypothesis assumed above will give roughly approximated results. Then we are allowed without wasting more calculations, to hypothesize a variation of n proportional to m.

The relation (5) is plotted in fig. 9b, for $c = 1$. For $j_0 < 0.9$ it is not necessary to impose critical damping conditions to assure stability to the circuit.

For $0.9 < j_0 < 0.99$ the values of K between the forbidden gap are cautelative because little overshoots may be allowed. This cannot be repeated for the values of K corresponding to $j_0 > 0.99$, being now important the contribution of noise.

5. Comparison with experimental results

We have examined many published results which are in agreement with our calculations, as can be seen from the following example:

Referring to [16]) we have verified the points on the diagrams in fig. 5–7. For fig. 6 (dead-time vs inductance) we find a satisfactory agreement, considering that in such figure the results are given for the 90% of the recovery time. For fig. 5 (output pulse width vs inductance) and fig. 7 (pulse height vs inductance) the behaviour is the same as in our fig. 3 and 6.

The absolute values are a little different on account of the fact that the monostables considered in [16]) are realised with gallium arsenide diodes loaded by a germanium diode that is a very heavy load[28]). Many experimental results, obtained with different types of td (GaAs and Ge, fast and slow types) and for several values of K have been compared with the expected results from the diagrams, showing an agreement within 10%.

The helpful assistance of Prof. M. Merlin and the encouragement of Prof. G. Giannelli are greatly acknowledged.

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